



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sheu, et al. Docket No.: TSM03-0140  
Serial No.: 10/619,828 Art Unit: 2811  
Filed: July 15, 2003 Examiner: TBD  
For: Self-Aligned MOSFET having an Oxide Region below the Channel

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IDS Forms PTO/SB/08a and 08b (3 pages) citing (41) references  
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Respectfully submitted,

A handwritten signature in black ink that reads "Natalie Swider".

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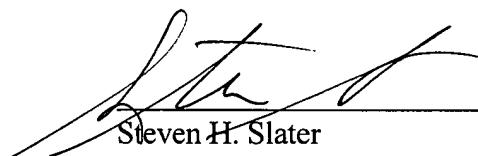
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No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

25 MAR 2004

Date



\_\_\_\_\_  
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MAR 29 2004

PTO/SB/08B (10-01)

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**Complete if Known**

Application Number	10/619,828
Filing Date	07/15/2003
First Named Inventor	Sheu, et al.
Group Art Unit	2811
Examiner Name	TBD
Attorney Docket Number	TSM03-0140

**OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	18	ISMAIL, K., et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.	
	19	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.	
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	22	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp.7-14.	
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	29	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.	
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	31	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	32	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
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	35	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
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	37	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
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	41	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.	
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